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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,771	12/02/2003	Arun Rao	15144US02	3834

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EXAMINER
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COLUCCI, MICHAEL C

ART UNIT	PAPER NUMBER
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2609

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/725,771	<b>Applicant(s)</b> RAO ET AL.	
	<b>Examiner</b> Michael C. Colucci	<b>Art Unit</b> 2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: **(See MPEP Ch. 2141)**

- a. Determining the scope and contents of the prior art;
  - b. Ascertaining the differences between the prior art and the claims in issue;
  - c. Resolving the level of ordinary skill in the pertinent art; and
  - d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.
2. Claims 1-3, 8, 10, 12-14, and 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Morton et al, us 2003/0163327, herein after Morton.

Re claim 12, "an integrated circuit for decoding audio data", Morton teaches a decoder in combination with a processor that performs decoding compressed audio stream data, (Morton, page 1 [0002]). Morton also teaches of a chip used to implement the invention, (Morton, page 3 {0027}).

"A controller", Morton also teaches a processor which will be representative of the common microcontroller, which is integrated, (Morton, Abstract). Having code stored within a memory for execution implies the use of integrated circuits.

"A memory connected to the controller", Morton teaches that a memory is arranged to store compressed data and decompression algorithms within the processor as part of the decoding apparatus, (Morton, page 1 [0004]).

"An instruction memory", Morton teaches executable instructions representing a computer program stored within memory, (Morton, page 1 [0006]). "A plurality of instructions", Morton teaches a program for performing the task of storing operating data and code for a plurality of decompression algorithms, (Morton, page 1 [0006]).

"Writing data corresponding to the first audio decoding function to the memory", Morton teaches a processor in combination with a decompression algorithm which together select and decode compressed data, (Morton, Abstract). Although Morton is silent on a "decoding function" per se, Examiner takes Official Notice that it is well known and therefore obvious that a decompression function defined within the scope of a computer program is necessary to decode encoded data, where a decompression function can relate to linearity or non-linearity and defined through various means, i.e. lookup table, matrices, etc. "Writing data corresponding to the second audio decoding function to at least a portion of the memory", Morton teaches that a plurality of decompression algorithms exist that require different amounts of memory, (Morton, Abstract, Claim 2). "Partially overwritten by data", Morton teaches that the processor and decompression algorithm combination are set to allocate an amount of memory for storing data. Allocation is broad and construed to mean that memory can be allocated through the overwriting of prior data, (Morton, page 1 [0004]).

Re claim 13, "grouped together", Morton teaches that there is a plurality of decompression algorithms present. "Grouping" is general as to be construed as being present within memory existing at the same time, (Morton, Abstract).

Re claim 14, "execution of the plurality of instructions by the controller causes performing of the audio decoding functions in an order based upon memory allocation", Morton teaches that the allocated portion of memory corresponds to a first and a second portion arranged for storage suitable for the decompression algorithms, (Morton, Claim 2). The order of selection of decompression algorithms will directly relate to the order of allocation of memory as a result.

Re claim 17, "audio decoding function is optimized to reduce memory used", Optimization is broad as to be construed as the improving of a systems performance. Morton teaches the implementation of a gateway packet voice exchange service (PVE), where the overall memory consumption is reduced though a low bit rate and various forms of memory available, (Morton, page 2 [0021]). Reducing memory consumption in this new manner is a form of optimization because it is an improvement of performance.

Claim 1 has been analyzed and rejected with respect to claim 12. Claim 1 is the method of the apparatus of claim 12.

Claim 2 has been analyzed and rejected with respect to claim 13. Claim 2 is the method of the apparatus of claim 13.

Claim 3 has been analyzed and rejected with respect to claim 14. Claim 3 is the method of the apparatus of claim 14.

Claim 8 has been analyzed and rejected with respect to claim 17. Claim 8 is the method of the apparatus of claim 17. Storing or writing data is part of the decoding process, (see analysis for claim 12).

Re claim 10, "performing a third audio decoding function", Morton teaches the method of the apparatus applied to claim 12, as a plurality of decompression algorithms exist that require different amounts of memory, (Morton, Abstract, Claim 2). "Partially overwritten by data", Morton teaches that the processor and decompression algorithm combination are set to allocate an amount of memory for storing data. Allocation is broad and construed to mean that memory can be allocated through the overwriting of prior data, (Morton, page 1 [0004]). The use of plurality suggests more than one use, therefore any number greater than one, such as a third use of the function is a plurality.

Claim 18 has been analyzed and rejected with respect to claim 12. Claim 18 is the system of the apparatus of claim 12. Also, "A minimum amount of memory", Morton teaches the reduction of overall memory consumption, (Morton, page 2 [0021]). Reducing memory is construed as a form of optimization, which would involve a system having a minimum amount of memory present.

Claim 19 has been analyzed and rejected with respect to claim 12. Claim 19 is the system of the apparatus of claim 12.

**3. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton et al as applied to claim 1 above and further in view of Houha et al, US 5,734,822 (herein after Houha).**

Re claim 4, “a minimum amount of memory” in a “particular group”, Morton teaches the allocation of memory through the use of a processor and decompression algorithm (see analysis for claim 12). However, Morton fails to teach of a minimum amount of memory used during the process of decoding. Houha teaches a loader that allocates only the minimum amount of separate areas instead of allocating a large area, (Houha Col. 8 line 18-27). A separate area indicates a particular area. Therefore, the combined teaching of Morton and Houha would have rendered obvious the allocation of minimum memory relative to a particular decoding process.

Re claim 5, “a minimum amount of memory” to perform “all audio decoding functions”, Morton teaches the allocation of memory through the use of a processor and decompression algorithm (see analysis for claim 12). However, Morton fails to teach of a minimum amount of memory used during the process of decoding. Houha teaches a loader that allocates only the minimum amount of separate areas instead of allocating a large area, (Houha Col. 8 line 18-27). A separate memory area, as disclosed by Houha is broad as to be construed as separate memory devices that are used during the dissemination of incoming data. “All audio decoding functions”, Morton teaches a plurality of decompression algorithms in unison with a processor that decodes data. Therefore, the combined teaching of Morton and Houha would have rendered obvious the allocation of minimum memory relative to an all-decoding process within a single memory device.

**4. Claims 6, 7, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton et al as applied to claim 1 and 13 above and further in view of Hewitt et al, US 5,809,466 (herein after Hewitt).**

Re claim 15, "A plurality of memory devices", Morton teaches memory within the system used for storage based on the processor and decompression algorithm combination. However, Morton fails to teach that a plurality of memory devices are connected to the controller. Hewitt discloses that the transferring of data between off-chip local memory devices and a separate synthesizer module exists, (Hewitt, Col. 171 line 38-48). Therefore, the combined teaching of Morton and Hewitt would have rendered obvious the integrated circuit used for storing data based upon memory allocation with an addition of multiple memory devices.

Claim 16 has been analyzed and rejected with respect to claim 13 and claim 15. The grouping of memory or memory devices is implied though the existence of a plurality of memory or memory devices.

Claim 6 has been analyzed and rejected with respect to claim 15. Claim 6 is the method of the apparatus of claim 15.

Claim 7 has been analyzed and rejected with respect to claim 16. Claim 7 is the method of the apparatus of claim 16.

**5. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton et al as applied to claim 1 above and further in view of Houha et al and Watkins, US 5,859,609.**



Re claim 9, "using a maximum amount of memory sufficient to perform an audio decoding function using a maximum amount of memory is allocated, and each audio decoding function is performed using less memory in the single memory device", Morton and Houha together teach the allocation of a minimum amount of memory applied to decoding through the use of a processor and decompression algorithms (see also rejections of claims 4-5). However, the combination of Morton and Houha as a whole fails to teach of a method where a maximum amount of memory is used while using less memory overall in the memory devices. Watkins teaches the allocation of memory segments during an entire duration of data transmission with minimum excess memory, (Col. 7 line 30-42). Memory segments is broad as to be construed as separate memory devices or partitioned memory within a single device itself. Therefore, the combined teaching of Morten et al, Houha et al, and Watkins would have rendered obvious a method for maximizing the maximum amount of allocated memory using less memory overall in memory.

Claim 11 has been analyzed and rejected with respect to claim 9. Claim 9 is more comprehensive as compared to claim 11, where maximum memory location is taught but reduction of memory is not (i.e. "using less memory").

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-20010029446, US-20030208359, US-6330644, US-5867819, and US-6885992.

***Examiner's Note***

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

***Contact***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Colucci whose telephone number is (571)272-1847. The examiner can normally be reached on 7:30 am - 5:00 pm , alt. Fridays. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571)-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for


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published applications may be obtained from either Private PAIR or Public PAIR.

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